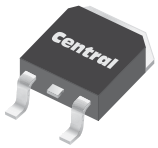
CJD13003

SURFACE MOUNT
NPN SILICON
POWER TRANSISTOR



DPAK TRANSISTOR CASE

Central Semiconductor Corp.

www.centralsemi.com

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CJD13003 type is an NPN Silicon Power Transistor manufactured in a surface mount package designed for high voltage, high speed power switching inductive applications.

MARKING: FULL PART NUMBER

MAXIMUM RATINGS: (T_C=25°C unless otherwise noted)	**SYMBOL**		**UNITS**
Collector-Emitter Voltage	V_{CEV}	700	V
Collector-Emitter Voltage	V_{CEO}	400	V
Emitter-Base Voltage	V_{EBO}	9.0	V
Continuous Collector Current	I_C	1.5	A
Peak Collector Current	I_{CM}	3.0	A
Continuous Base Current	I_B	750	mA
Peak Base Current	I_{BM}	1.5	A
Continuous Emitter Current	I_E	2.25	A
Peak Emitter Current	I_{EM}	4.5	A
Power Dissipation	P_D	15	W
Power Dissipation (T_A=25°C)	P_D	1.56	W
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	°C
Thermal Resistance	Θ_{JC}	8.33	°C/W
Thermal Resistance	Θ_{JA}	80.1	°C/W

ELECTRICAL CHARACTERISTICS: (T_C=25°C unless otherwise noted)

SYMBOL	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
I_{CEV}	V_{CE}=700V, $V_{BE(off)}$=1.5V			100	μA
I_{CEV}	V_{CE}=700V, $V_{BE(off)}$=1.5V, T_C=100°C			2.0	mA
I_{EBO}	V_{EB}=9.0V			1.0	mA
BV_{CEO}	I_C=10mA	400			V
$V_{CE(SAT)}$	I_C=500mA, I_B=100mA			0.5	V
$V_{CE(SAT)}$	I_C=1.0A, I_B=250mA			1.0	V
$V_{CE(SAT)}$	I_C=1.5A, I_B=500mA			3.0	V
$V_{CE(SAT)}$	I_C=1.0A, I_B=250mA, T_C=100°C			1.0	V
$V_{BE(SAT)}$	I_C=500mA, I_B=100mA			1.0	V
$V_{BE(SAT)}$	I_C=1.0A, I_B=250mA			1.2	V
$V_{BE(SAT)}$	I_C=1.0A, I_B=250mA, T_C=100°C			1.1	V
h_{FE}	V_{CE}=2.0V, I_C=500mA	8.0		40	
h_{FE}	V_{CE}=2.0V, I_C=1.0A	5.0		25	
f_T	V_{CE}=10V, I_C=100mA, f=1.0MHz	4.0			MHz
C_{ob}	V_{CB}=10V, I_E=0, f=0.1MHz		20		pF

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CJD13003

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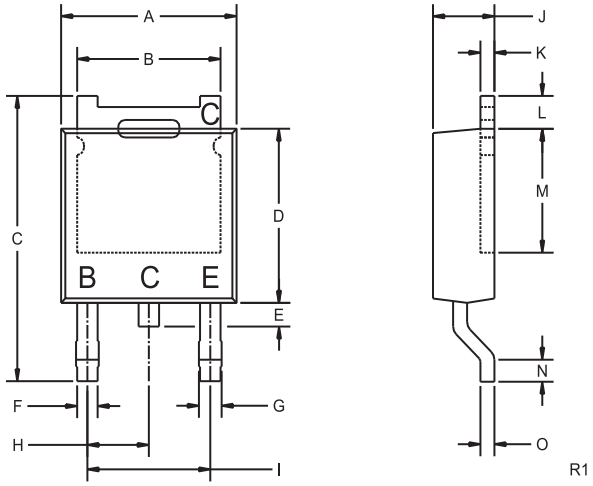
ELECTRICAL CHARACTERISTICS - Continued: (T_C=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
t_d (Note 1)	V_{CC}=125V, I_C=1.0A, I_{B1}=I_{B2}=200mA		0.1	μs
t_r (Note 1)	V_{CC}=125V, I_C=1.0A, I_{B1}=I_{B2}=200mA		1.0	μs
t_s (Note 1)	V_{CC}=125V, I_C=1.0A, I_{B1}=I_{B2}=200mA		4.0	μs
t_f (Note 1)	V_{CC}=125V, I_C=1.0A, I_{B1}=I_{B2}=200mA		0.7	μs

Notes (1) tp=25μs, Duty Cycle≤1%

DPAK TRANSISTOR CASE - MECHANICAL OUTLINE



DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.250	0.265	6.35	6.73
B	0.205	0.215	5.21	5.46
C	0.374	0.409	9.50	10.40
D	0.235	0.245	5.97	6.22
E	0.025	0.040	0.64	1.02
F	0.025	0.035	0.64	0.88
G	0.030	0.045	0.76	1.14
H	0.090		2.28	
I	0.180		4.57	
J	0.086	0.094	2.19	2.38
K	0.018	0.023	0.46	0.58
L	0.040	0.050	1.02	1.27
M	0.170	-	4.32	-
N	0.020	-	0.51	-
O	0.018	0.023	0.46	0.58

DPAK TRANSISTOR (REV: R1)

LEAD CODE:
B) BASE
C) COLLECTOR
E) EMITTER
C) COLLECTOR

MARKING:
FULL PART NUMBER

R2 (4-January 2010)