

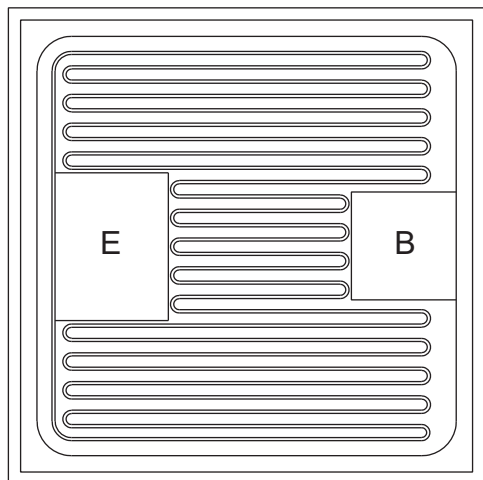
PROCESS CP309
Power Transistor
NPN - Low Saturation Transistor Chip



PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	41.3 x 41.3 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	9.4 x 9.2 MILS
Emitter Bonding Pad Area	12.8 x 10.2 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Ag - 12,000Å

GEOMETRY



BACKSIDE COLLECTOR R1

GROSS DIE PER 4 INCH WAFER

6,285

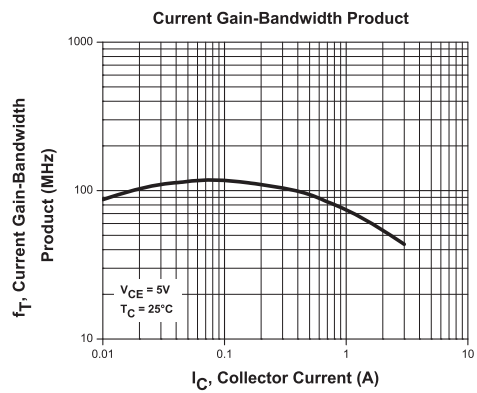
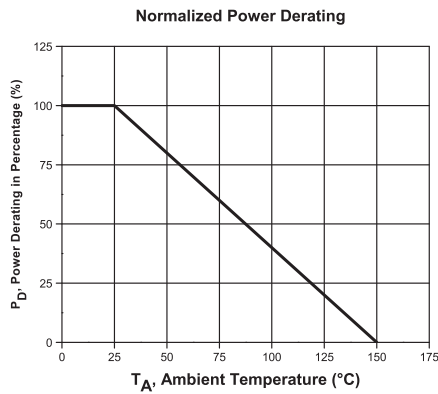
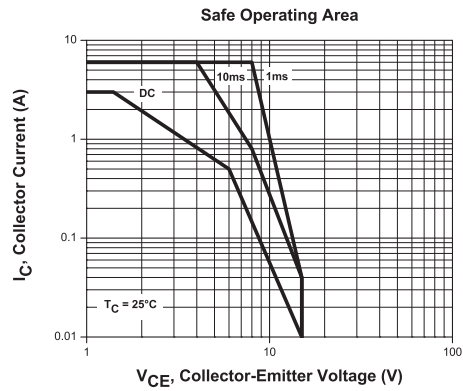
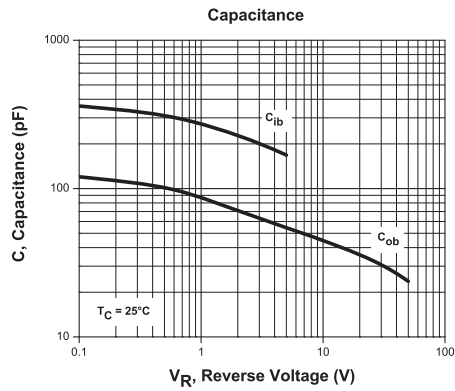
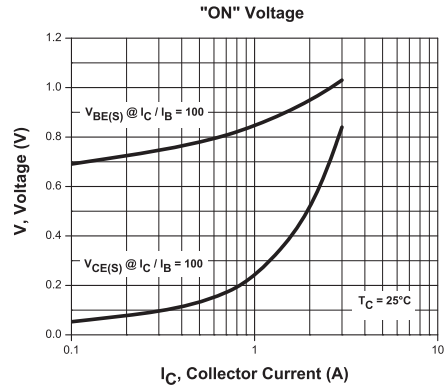
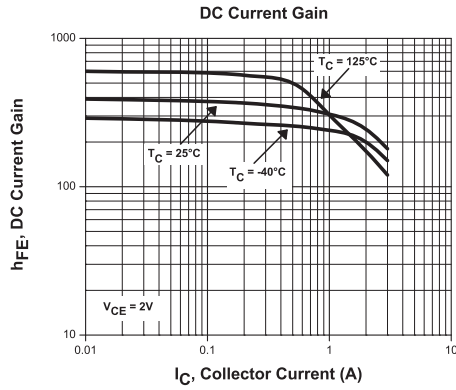
PRINCIPAL DEVICE TYPES

- CXT3090L
- CZT3090L
- CMXT3090L

R5 (16-December 2011)

PROCESS CP309

Typical Electrical Characteristics



R5 (16-December 2011)