

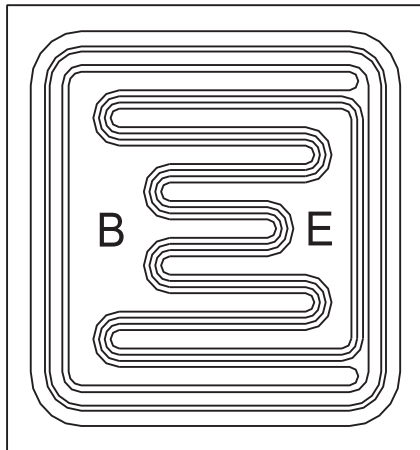
PROCESS CP208
Power Transistor
NPN - Amp/Switch Transistor Chip



PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	66 x 66 MILS
Die Thickness	12.5 ± 1.0 MILS
Base Bonding Pad Area	12 x 24 MILS
Emitter Bonding Pad Area	11 x 14 MILS
Top Side Metalization	Al - 50,000Å
Back Side Metalization	Cr/Ni/Ag - 16,000Å

GEOMETRY



BACKSIDE COLLECTOR

GROSS DIE PER 4 INCH WAFER

2,630

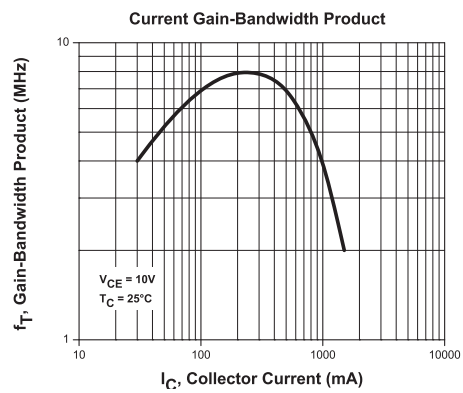
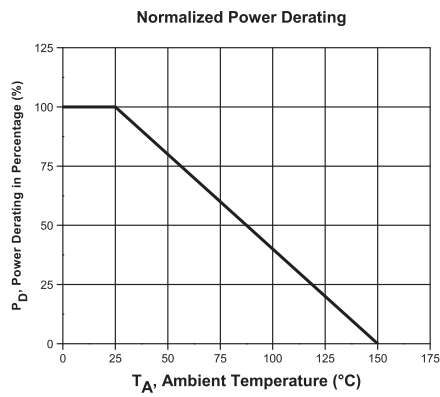
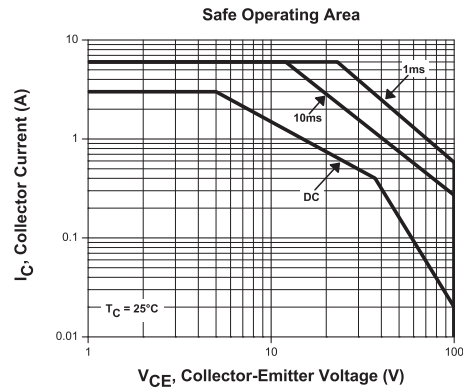
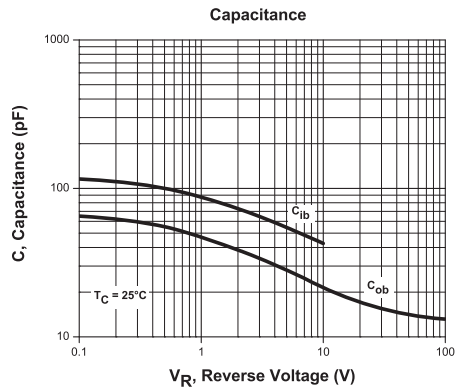
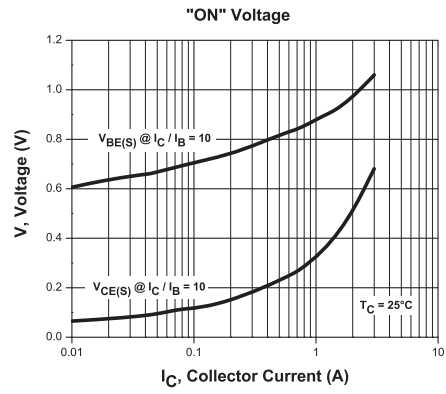
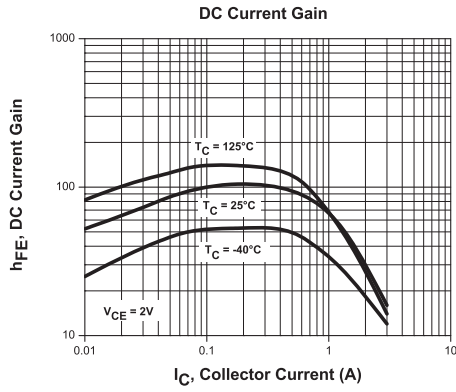
PRINCIPAL DEVICE TYPES

CJD31C
MJE182
TIP31C

R4 (22-March 2010)

PROCESS CP208

Typical Electrical Characteristics



R4 (22-March 2010)